

BWS-2010 INTELLIGENT VIDEO CARD

BWS-2011 INTELLIGENT COLOUR VIDEO CARD

TECHNICAL MANUAL

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1. INTRODUCTION

1.1. General

The BWS-2010 Intelligent Video Display Card provides a complete video display subsystem for the STD BUS, which can function as anything from a high performance CRT terminal to a separate co-processing display subsystem. The card is organised around an on-board Z80 microprocessor and a 6845 CRT controller chip, and is designed to allow full speed Z80 program execution with a minimum of wait states. In particular, the card allows continuous access to the video memory from the on-board Z80 with NO flicker or spurious images, and supports extremely fast rates of data transfer to and from the host computer (in excess of 30 kbyte/sec in burst mode).

The card is installed inside the host computer system card cage, and requires an external video monitor and a parallel ASCII keyboard to make a complete display subsystem.

1.2. Summary of Features

- . The video display is generated using a 6845 CRT controller. Hence the standard display size of 80 x 24 characters may be re-arranged as desired by the user.
- . The standard character set comprises all 96 printable ASCII characters, together with 32 semi-graphical characters for special effects (such as table borders). Characters are based on a 7x9 matrix in a 8x12 region. With a larger character generator (16 kbyte EPROM/RAM), a further 896 semi-graphical characters can be defined.

Reduced matrix characters (6x7 in a 7x9 region) are installed when the card is configured for 200 line VDU monitors (IBM PC compatible).

- . All display characters have independant attributes to specify one of eight brightness levels, flashing, inverse and underline.
- . For the BWS-2011 colour card, the display attributes are used to select 1 of 8 foreground colours, 1 of 4 background colours and flashing, on a per character basis. Colours may be defined from a palette of 16 colours when using TTL colour VDU's or from 4096 colours when analogue colour VDU's.
- . Using a RAM based character generator, graphic displays with a resolution of 640 x 300 pixels may be created by the host computer, built up from software generated semi-graphic characters. Full bit mapped graphics can be generated at a resolution of 512 x 256 pixels.

- . An on-board Z80A interfaces between the display generator and the host computer. The Z80A may be programmed to emulate most CRT terminals. Software for an enhanced Lear Seigler ADM-31 is stored in EPROM. However the card is arranged so that Z80A software may be down-loaded from the host computer and stored in RAM. Thus the user may create individualised CRT terminals.
- . The video display memory is fully dual ported between the CRTC display generator and the on-board Z80 processor, to allow display update to occur at any time without flicker. This allows rapid screen update and manipulation with absolutely no flicker.
- . ByteWyde Systems BWS-1000 Z80 monitor program can be included into the on-board Z80 software to debug down-line loaded programs. Individual terminal emulations or video co-processing procedures thus can be easily developed.
- . ByteWyde Systems BWS-1150 Enhanced Command Basic can be included into the on-board Z80 software to create a simple co-processing environment. Video displays can be programmed on-card entirely in Basic, with the STD BUS being treated as a high speed remote data port for receiving and sending information.
- . A 64 byte keyboard type-ahead buffer, and a 256 byte host computer communication buffer is included in the EPROM software.
- . All RAM and EPROM sockets are designed to accept both 24 and 28 pin JEDEC standard memory chips, to allow Z80A software, number of character sets and video memory size to be increased if desired.
- . 256 bits of EEPROM are available to permanently store terminal setup characteristics.
- . The BWS-2010 Intelligent Video Display Card interfaces to the host computer as if it were a conventional serial interface. However as the interface is in fact parallel, burst data transfer rates of better than 30 kbytes/second may be achieved until the card's communication buffer is filled.

1.3. Colour Card (BWS-2011)

The BWS-2011 Intelligent Colour Video Card is an enhanced version of the standard BWS-2010 Intelligent Video Card which replaces the black and white attributes of grey levels, underline and reverse, with both foreground and back ground colour selection for each character displayed. Characters may be selected to be displayed in one of eight foreground colours, with one of a separately definable four background colours. A separate cursor colour may be defined for each background colour.

Each foreground, background and cursor colour may be selected from a palette of 4096 colours. Up to eight foreground colours, four background colours and four cursor colours may be active at the same time. Colours may only be reprogrammed during the vertical retrace period of the display.

As with the monochrome card, colour bit mapped graphics may be achieved to a resolution of 640 x 300 pixels using character cells of 8 x 12 with software generated semi-graphics characters. Full bit mapped graphics may be generated to a resolution of 512 x 256 pixels (character cells of 8 x 16) by using 62256 RAM for the character generator. The only limitation is that the colour must be defined on a per character cell basis, not on a pixel basis.

1.4. Hardware Overview

The card has 16 kbytes of EPROM and up to 16 kbytes of RAM available for internal use by the Z80 processor. Another 32 kbytes of RAM are dual ported with the 6845 controller on a cycle interleave basis (for maximum speed of video update) to provide up to 8 kbytes of video character RAM, 8 kbytes of video attributes RAM and up to 16 kbytes of programmable character generator RAM (8 sets of 128 characters). Character attributes include 8 levels of brightness, flashing, inverse and underline for the monochrome card (BWS-2010); and 8 foreground colours, 4 background colours and flashing for the colour card (BWS-2011). Character set selection is done on an individual character basis using 2 video attribute bits. The card operates from a single 5V supply, and draws 1.3 A dc, approx.

A further 256 bytes of non-volatile EEPROM storage can be supplied with the card to save special setup parameters or other details.

The display structure is 80 x 24 characters, with a 25th status line available if necessary. Displayed characters are designed around an 8 x 12 matrix pattern, using the programmable character generator RAM. Semi graphic displays can be easily developed by creating new character sets on a host computer and downline loading them into the video card. Revised display structures can be achieved by reprogramming the 6845 controller and possibly changing the card crystal. Large display characters can be drawn by using semigraphic character sections, with appropriate onboard Z80 software. Alternatively, for display structures of less than 64 x 16 characters, a full bitmapped display can be implemented (512 x 256 pixels) by dedicating one of the possible 1024 semigraphic characters to each screen character position. Software for this application is available as an option.

The monochrome card provides a composite video output (TTL and 75 ohm) with separate sync signals if required. The color card provides 4 TTL color drive outputs (RGB and intensity) with separate sync signals. All sync signals may be +ve or -ve logic. Optionally, analogue color drive outputs may be provided (1V to 2V, black to full intensity).

A full 8 bit parallel keyboard interface is provided, with a separate BELL signal line. This interface directly suits APPLE compatible parallel keyboards. Also, an external synchronising INPUT is provided to allow the display to be locked to an external 50 Hz reference signal to avoid display ripple, or to an external vertical sync signal to lock to external video.

The card appears on the STD BUS interface as 4 I/O ports. Two of these ports are used as data and control ports, similiar to a conventional UART. A third port is used to store an interrupt vector. The BWS-2010 and BWS-2011 cards fully support interrupts on data flowing to and from the card. Interrupts may be vectored or unvectored, and the card supports the STD BUS interrupt priority structure through PCI and PCO. Particular care has been taken to ensure that multiple BWS-2010 cards can operate using prioritised Z80 mode 2 vectored interrupts on one motherboard, to allow multiple display to be supported in one system.

The card may be used in a wide variety of applications. The standard software supplied with the card emulates an ADM3A Lier-Seglier terminal, with enhancements. Other terminal emulations are available, and may be downline loaded into the card online if required. Support software is also available for users to develop their own terminal emulations or other software.

The card can also function as a co-processing display subsystem, executing a program separately from the main STD BUS host processor to generate displays in real-time. ByteWyde Systems BWS-1000 Z80 monitor program and BWS-1100 Command Basic can be supplied to execute in the card, to assist with the development of such co-processing software programs.

1.5. Software Overview

Software supplied with the video card emulates an ADM3A Lier-Seglier terminal, with enhancements. The software supports a 256 byte bi-directional typeahead buffer to the STD BUS, and a 64 byte typeahead buffer from the keyboard. Larger buffers can be supplied on request. Typeahead buffers or interrupt driven terminal handlers on the host computer are NOT required with this system. The terminal emulation software requires approx 4 kbyte of Z80 EPROM and 1 kbyte of Z80 RAM. The remaining Z80 memory space is available for user programs.

Enhancements to the terminal emulation include additional escape sequences to invoke the extra video attributes of the card, the selection of alternate character sets and the loading of INTEL HEX files through the bus interface. (This allows alternative character sets or user emulation/application programs to be loaded into the card from a host computer). The terminal emulation software is highly modular, with well defined jump table entries into all useful subroutines. User written programs can therefore avoid the effort of screen management and effectively output to a very fast terminal.

For program development on card, a BWS-1008 high performance monitor program can be supplied in EPROM. This monitor allows a user to read and write to oncard memory or ports, fill memory, load program or displays from the STD BUS, or to execute user programs with software breakpoints. User programs can also be down-line loaded into the card with this monitor.

For co-processing applications, ByteWyde Systems Enhanced Command Basic (multitasking) can be supplied in EPROM oncard. This software allows display generation routines to be written and executed in interpretative BASIC with minimal overhead to the host processor on the STD BUS. In effect, the bus becomes a data transfer route between the host processor and the slave processor on the video card. The implementation of Command Basic on the video card is fully compatible with other versions of this product, allowing Basic programs to be developed and stored elsewhere and down-line loaded to the card when required.

Two support packages are also available for either CP/M or MS-DOS computer systems. A font editor can be supplied to assist with the creation of custom character sets, and a loader program is available to facilitate the transfer of programs, displays or character sets from a host processor to a video card.

In summary, the BWS-2010 Intelligent Video Display Card provides a powerful and flexible CRT terminal capability at a greatly reduced cost. All the major facilities may be re-arranged under user control, allowing the card to be used in a wide variety of applications.

2. TECHNICAL SPECIFICATION

2.1. Video Section

Video Outputs: 75 ohm Composite Video
(BWS-2010 Easily adaptable to TTL video (no sync)
monochrome) Horizontal and Vertical sync (+ve and -ve logic)
Composite Sync (-ve logic)

Video Outputs: TTL RGB and intensity signals
(BWS-2011 Optional 1V-2V RGB analogue video
colour) Horizontal and Vertical sync (+ve and -ve logic)

Display Generator: Motorola 6845 CRT Controller

Video Memory: 2 kbyte RAM (6116 or equivalent)
Expandable up to 8 kbyte (4 display pages)

Attributes Memory: 2 kbyte RAM (6116 or equivalent)
Expandable up to 8 kbyte

Attributes per character comprise character set selection, 1 of 8 grey levels, blink, reverse and underline.

Colour attributes comprise 1 of 8 foreground colours, 1 of 4 background colours, 1 of 4 cursor colours, blink.

Programmable

Character Generator: 2 kbyte RAM (6116 or equivalent)
Expandable up to 16 kbyte of EPROM/RAM (62256/27128 or equivalent) - 1024 characters

All video memory is fully dual ported between the CRTC and the on-board Z80 using interleaved cycle sharing, with wait state synchronisation for the Z80 processor.

Keyboard Interface: 8 bits parallel ASCII, with strobe (+ve or -ve logic). Separate BELL and RESET output.

Synchronise Input: TTL level synchronising input to allow 6845 to synchronise to external video or 50 Hz signal

2.2. On-Board Processor Section

Processor: 3.38 MHz Z80A microprocessor. No wait states except when accessing video memory.

Processor Memory: 8 kbyte of EPROM memory (2764 or equivalent)
Expandable up to 16 kbyte (27128 or equivalent)

2 k byte of RAM memory (6116 or equivalent)
Expandable up to 16 kbyte (62256 or equivalent)

256 bits of EEPROM memory (NMC9306)

Reset: Hardware reset from STD BUS
NMI reset from pushbutton on card

2.3. STD BUS Interface

STD BUS I/O Address Space: 4 ports decoded, link selectable to anywhere in STD BUS I/O space (even address boundary). IOEXP is decoded. Default address is at B0 hex.

BWS-2010 card appears as ordinary UART to host processor on the STD BUS.

Interrupts: Z80 Mode 1 or 2 vector interrupts supported on the STD BUS. Interrupts on byte receipt or transmission to the STD BUS may be separately mask enabled by host software.

On-board Z80 STD BUS Interface: Z80A PIO, operating in mode 2 interrupt to on-board Z80 processor.

2.4. Software

Standard Emulation: Modified ADM31 Lier Seglier Terminal

Other standard emulations available on request

Support Software Available: BWS-1000 Z80 Monitor
BWS-1100 Command Basic
CP/M Font Editor Utility Program
CP/M Down-line Loader Utility Program

2.5. General

Physical Dimensions: 4.5 inches x 7.3 inches (BWS-2010 mono version)
4.5 inches x 7.8 inches (BWS-2011 colour version)
Card is notched at 6.5 inches to fit card ejector.

Power Requirements: 5 volts, 1.4 A approx

Bus Compatiblity: Fully compatible with all STD BUS
specifications, including component height.

Environmental: 0 - 50 °C free air temperature
5% - 95% non condensing humidity

Warranty: 3 months. All units are tested for 24 hours at
ambient temperature and 2 hours at 45 °C to
minimise infant mortality.

3. OPERATION

3.1. Installation and Setup

3.1.1. General

The BWS-2010 Intelligent Video Card is supplied complete and ready for operation. The card only requires connection of a VDU monitor and keyboard.

The standard memory configuration for the card is 8 kbytes of Z80 EPROM, 2 kbytes of Z80 RAM, 2 kbytes of Video and Attributes RAM and 2 kbytes of PCG RAM. Links on the card can be used to select alternative memory configurations. Refer to section 3.3 for details.

Other memory configurations can be supplied on request at time of order on a cost plus basis.

Standard software comprises a extended ADM31 terminal emulation. Other terminal emulations can be supplied on request at no extra charge. The card can also be supplied with an on-board monitor (BWS-1008 Z80 monitor) for debugging user programs, or with on-board Enhanced Command Basic (BWS-1158) for developing co-processing display systems. These software additions are available as field installable options after purchase of the card.

3.1.2. Video Output

The BWS-2010 monochrome card provides a variety of video output options. The standard output is composite video, comprising -ve logic horizontal and vertical sync pulses anded together with the video signal. This output conforms to RS-170 standard, with the video level varying from 1V to 2V and sync pulses being at 0V (from 1V threshold). Separate sync pulses are also available at the card edge video connector as positive logic signals. For monitors which require TTL video with -ve logic sync pulses, additional components can be added to the video card to invert the normally positive logic sync pulses. Refer to section 3.3 for details.

The BWS-2011 colour card provides a similar variety of output options. The standard output is separate TTL colour drive signals (RGB and intensity) with separate +ve logic horizontal and vertical sync pulses. The sync pulses can be inverted to -ve logic using links on the card. Analogue colour output (RGB) in the range 1V to 2V can be provided by adding additional components to the card. Composite sync can be mixed with any analogue colour output if required. Refer to section 3.3 for details.

The monochrome video output levels have been preset on the card before delivery. However, some adjustment may be required to suit individual CRT monitors. This can be done as follows:

The sync threshold level for composite video can be adjusted using RV2. If an oscilloscope is available, the threshold should be set to 1V, and adjusted from there until the monitor locks solidly. Otherwise simply adjust RV2 until sync is achieved.

RV1 adjusts the video brightness. It has most effect on the lowest video brightness level. Trim RV1 to obtain a balanced range of brightness levels for your particular CRT monitor.

NOTE: With some CRT monitors, the brightness level variations achieved using the video card may need adjustment. This can be done by varying resistors R1, R2, R3 on the card. These resistors act as a -ve logic OR gate, to achieve 8 brightness levels. Consult the circuit diagram for more detail.

There are no trim adjustments available for the BWS-2011 colour card.

Non standard video output combinations can be configured before delivery if requested at time of order at no extra charge.

Video Connector (J2) pinouts are shown in Figure 3-1. Refer to Appendix C for the location of the video connector and the components discussed above.

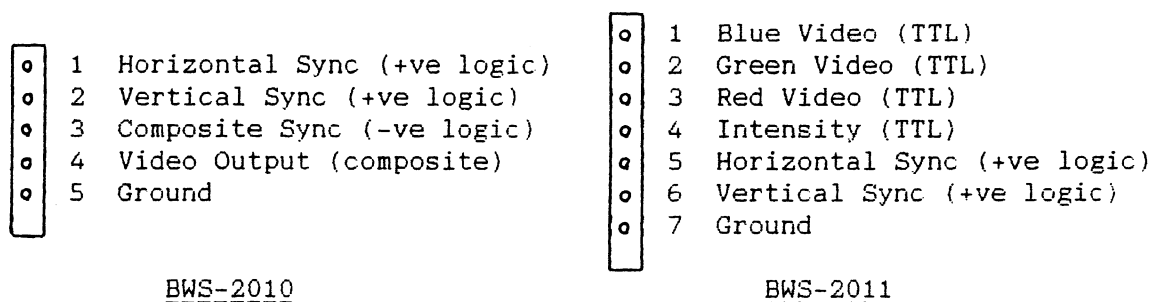


Fig. 3-1: Video Connector Outputs (J2)

3.1.3. Keyboard Interface

The standard keyboard arrangement on the card provides a standard 8 bit parallel ASCII interface, requiring a +ve edge strobe pulse from the keyboard for the internal latch on the card. A -ve edge strobe pulse can be accepted by reversing a link on the card. Refer to section 3.3 for details.

The keyboard interface also provides a 5V power takeoff, and a separate Power On Reset and Bell output signal. The Bell signal is directly controlled by the on-board microprocessor through its PIO, and may be used for any purpose.

Keyboard Connector (J1) pinouts are shown in Figure 3-2. Refer to Appendix C for the location of the keyboard connector.

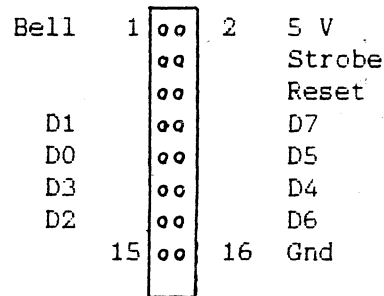


Fig. 3-2: Keyboard Connector Pinouts (J1)

3.1.4. STD BUS Interface

The BWS-2010 Intelligent Video Card occupies 4 out of the available 512 I/O address locations available on an 8 bit STD BUS system (8 address bits plus IOEXP). Extended I/O addressing to 16 address bits is NOT supported by the BWS-2010. The 4 video card ports must be located on an even 4 port boundary in the STD BUS I/O address space. The default base I/O address for the BWS-2010 card is B0 hex, and this base address must be used when the card is used as the display console for any of ByteWyde Systems software products. Other card base addresses may be implemented by changing links oncard. Refer to section 3.3 for details.

The port address usage for the card and bit allocation for the Control/Status port are illustrated in Figure 3-3.

BASE + 0	8 bit Data Port	R/W
BASE + 1	Control/Status Port	R/W
BASE + 2	Interrupt Vector Port	R/W

CONTROL/STATUS PORT BITS

Bit 0 R/O	Rx Ready	Set when the card has an 8 bit data word to send to the STD BUS (usually a character from the keyboard).
Bit 1 R/O	Tx Ready	Set when the card is ready to accept an 8 bit data word from the STD BUS (usually an ASCII character).
Bit 2 R/W	Rx Int Enab	Enables an INTRQ interrupt to occur when Rx Ready (bit 0) is set.
Bit 3 R/W	Tx Int Enab	Enables an INTRQ interrupt to occur when Tx Ready (bit 1) is set.
Bit 5 R/O	Card Busy	Set when the card is busy processing data and cannot accept data from the STD BUS.

Fig. 3-3: STD BUS I/O Port Interface

NOTE: For normal terminal operation, host computer software should ensure that Bit 1 of the Control/Status port is "1" and that Bit 5 is "0", before sending a data byte to the video card.

However, in detail, Bit 1 indicates that a data byte has been accepted by the interrupt service routine in the on-board Z80 processor, while Bit 5 indicates that the on-board processor cannot at present process a data byte which may have been accepted by the interrupt service routine. This arrangement is adopted so that the on-board processor may be interrupted from lengthy processing at the interrupt level, and gracefully reset by an appropriate control command. Refer to section 5.2 for further details.

3.1.5. External Sync

The BWS-2010 video card can be exactly synchronised to 50 Hz or to external video by connecting a 50 Hz or vertical sync pulse to connector J3. 50 Hz external sync minimises display ripple due to external fields, while an external vertical sync pulse allows video output from the card to be mixed with other video signals. The external sync pulse must be -ve logic and have a minimum duration of 1 microsecond.

Note that this option for the video card should be specified at the time of purchase, since a software variation is required to correctly set up the 6845 CRTC chip for external synchronising.

Sync Connector (J3) pinouts are shown in Figure 3-4.

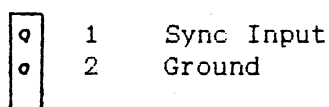


Fig. 3-4: Sync Connector (J3) Pinouts

3.2. Software

The BWS-2010 Intelligent Video Card is normally supplied with a enhanced ADM31 terminal emulation, or with a purchaser requested alternative terminal emulation. However, for applications where the card is to be programmed with user generated software, two software alternatives are available.

The card can be supplied with BWS-1008 Z80 monitor program on the card. This allows user developed software to be easily loaded into the video card, and provides excellent debugging support.

Alternatively, the card can be supplied with BWS-1158 Enhanced Command Basic on the card. This provides an easy on-card display processing capability, using the STD BUS as a high speed data transfer port. Command Basic is particularly useful to rapidly develop special screen formats, especially where semi-graphic character manipulation is involved.

Manuals for BWS-1008 and BWS-1158 are not normally supplied with the video card product and must be separately ordered when required.

3.2.1. ADM31 Terminal Emulation

The standard BWS-2010 terminal emulation is a modified ADM31, with enhancements to take account of the extra capability of the BWS-2010 video card. All 96 printing ASCII characters are available as displayable characters, with a further 32 semi-graphic characters available through escape sequence selection.

Control characters and escape sequences for the enhanced ADM31A emulation are listed in Figures 3-5, 3.6 and 3.7.

control ^	Cursor home
control G	Ring keyboard bell
control H	Cursor left one character
control J	Cursor down one line
control K	Cursor up one line
control L	Cursor right one character
control M	Cursor to start of line
control Z	Clear screen

Fig. 3-5: ADM31 Emulation: Control Characters

BWS-2010/BWS-2011 Intelligent Video Card

ESC (1)	Select video brightness 0	ESC T	Erase to end of line
ESC (2)	Select video brightness 1	ESC *	Clear to end of screen
ESC (3)	Select video brightness 2	ESC v	Clear Screen
ESC (4)	Select video brightness 3	ESC E	Insert line
ESC (5)	Select video brightness 4	ESC R	Delete line
ESC (6)	Select video brightness 5		
ESC (7)	Select video brightness 6		
ESC (8)	Select video brightness 7		
ESC <	Dim video on	ESC m	Cursor OFF
ESC (	Normal video brightness	ESC #	Display ON
ESC)	Bright video on	ESC \$	Display OFF
ESC {	Underline off	ESC x	Cursor ON
ESC }	Underline on		
ESC [	Inverse video off		
ESC]	Inverse video on		
ESC :	Flashing video on		
ESC ;	Flashing video off		
ESC H	Cursor Home	ESC 0	Select character set 0
ESC A	Cursor Up	ESC 1	Select character set 1
ESC B	Cursor Down	ESC 2	Select character set 2
ESC C	Cursor Right	ESC 3	Select character set 3
ESC D	Cursor Left	ESC g nnnn	Jump to Address nnnn
ESC = Y X	Direct cursor addressing	ESC h	Hex load

Fig. 3-6: ADM31 Emulation : Escape Sequences (BWS-2010)

ESC (1)	Select foreground colour 0	ESC T	Erase to end of line
ESC (2)	Select foreground colour 1	ESC *	Clear to end of screen
ESC (3)	Select foreground colour 2	ESC v	Clear Screen
ESC (4)	Select foreground colour 3	ESC E	Insert line
ESC (5)	Select foreground colour 4	ESC R	Delete line
ESC (6)	Select foreground colour 5		
ESC (7)	Select foreground colour 6		
ESC (8)	Select foreground colour 7		
ESC (9)	Select background colour 0	ESC m	Cursor OFF
ESC (A)	Select background colour 1	ESC #	Display ON
ESC (B)	Select background colour 2	ESC \$	Display OFF
ESC (C)	Select background colour 3	ESC x	Cursor ON
ESC :	Flashing video on		
ESC ;	Flashing video off		
ESC H	Cursor Home	ESC 0	Select character set 0
ESC A	Cursor Up	ESC 1	Select character set 1
ESC B	Cursor Down	ESC 2	Select character set 2
ESC C	Cursor Right	ESC 3	Select character set 3
ESC D	Cursor Left	ESC g nnnn	Jump to Address nnnn
ESC = Y X	Direct cursor addressing	ESC h	Hex load
		ESC c	Hex load to Color RAM

Fig. 3-7: ADM31 Emulation: Escape Sequences (BWS-2011)

3.2.2. VT52 Emulation

Not complete at time of printing

3.2.3. VT100 Emulation

Not complete at time of printing

3.2.4. On-Board Monitor (BWS-1008)

The BWS-1008 monitor is a special version of ByteWyde Systems Z80 monitor program, configured specifically for the BWS-2010 video card. Most standard monitor functions are available, including access to memory and CPU register variables, direct I/O manipulation, software breakpoints, NMI interruption of infinite loops, etc. The monitor treats the STD BUS as its remote port, and hence user software may be down-line loaded from the STD BUS into the video card with the normal monitor "L" function. Also, there is a special "Absolute Terminal" function which allows the video card to function as a normal terminal, and a "Send to Video" function which acts like a normal terminal in LOCAL mode.

For the BWS-2011 Colour video card, the BWS-1008 monitor program waits for the vertical retrace whenever the colour selection RAM is accessed by monitor command. The user can therefore directly set up colour combinations by simple monitor "port out" commands. (The subroutine used to achieve this waited store is available to user programs through the video jump table, see section 5.2)

The BWS-1008 monitor jump table is installed at address 080h (the same as the standard BWS-1000 monitor program) and monitor subroutines can be called from user programs as required through this jump table. Refer to the BWS-1000 Z80 Monitor manual for details.

The BWS-1008 monitor uses the underlying terminal emulation supplied with the card to access the screen and keyboard, and subroutines to access the terminal emulation are available through a jump table starting at location 0100h. Refer to Sections 4.3 and 5.2 for details.

Using the BWS-1008 Z80 monitor program, revised terminal emulations or user written display programs may be readily loaded from the host STD BUS processor and debugged as required.

3.2.5. On-Board Command Basic (BWS-1158)

BWS-1158 Enhanced Command Basic on the video card provides a complete alternative method of creating video displays. The Command Basic implementation allows a Basic program to periodically refresh background displays, receive and process information from the STD BUS, regularly update foreground displays and develop specific display formats quickly and easily. Command Basic provides a rapid technique to satisfy almost any display requirement, WITHOUT loading the host processor on the STD BUS. Refer to the BWS-1100 Command Basic users manual for more detail on ByteWyde Systems Enhanced Command Basic package.

In essence, Command Basic on the video card creates a true co-processing environment. The host STD BUS processor no longer has to send a string of ASCII characters to create a display picture. Rather, the data which is used to assemble a display picture can be sent to the video card and the conversion of this data to a displayed set of ASCII characters is done within the video card. Multiple displays can be created using a separate video card for each display, and the host processor need only send limited information to each video card to update particular displays. Additionally, a number of picture formats can be retained within a video card, and selected for display without the host processor being aware of the process. This technique of programming is particularly powerful when semi-graphic characters must be created at run-time to satisfy a particular display requirement. Refer to Sections 5.2 and 5.3 for more details of this use of the video card.

3.3. Options

3.3.1. Link Selection Summary

There are a number link headers on the BWS-2010 and BWS-2011 Intelligent Video Cards. The location of the link headers are shown on the Component Layout Diagrams in Appendix C. The link selectable options available are illustrated in Figure 3-8.

3.3.2. TTL Video Output : BWS-2010

The BWS-2010 Intelligent Video Card may be easily modified for TTL video output with separate sync pulses. The modification involves minor component re-arrangement to achieve TTL video output, and some additional components inserted if -ve logic separate sync pulses are required.

TTL video output on pin 4 of connector J2 is achieved by the following component re-arrangement:

- Remove variable trim pot RV2 (2k2)
- Short circuit Diode D4
- Replace Resistor R5 (470 ohm) with 4k7, 1/4 watt
- Cut pcb track link P1 (removes sync from video signal)

Trim pot resistor RV1 can be used to adjust the lower brightness levels as with composite video output. However, brightness levels for TTL monitors are often not as even as with composite video monitors, because of non-linear input circuitry, and the brightness control resistors (R1,R2,R3) may sometimes need adjustment for TTL levels. Also, some monochrome TTL monitors just cannot support variable intensities, and in these cases only a single intensity display can be achieved.

Negative logic sync pulses require the addition of one PN2222 transistor, one 4k7 and one 2k2 resistor, per sync pulse to be inverted. These components are installed under where trim pot RV2 was installed, as shown in Figure 3-9. Two 2 pcb track links per sync pulse to be inverted must also be cut, as shown.

3.3.3. Analogue Colour Output : BWS-2011

Section not available at time of printing

BWS-2010/BWS-2011 Intelligent Video Card

<u>Link</u>	<u>Purpose</u>	<u>Supplied as</u>	<u>Alternatives</u>	
W1	Connect Card Interrupt line to INTRQ on STD BUS	o o not connected	o—o connected	
W2	Define bit 1 of interrupt vector byte.	o o o not defined	o—o o bit set by card	o o—o bit set by host
W3	STD BUS I/O Port Address Selection Link Inserted means bit low Default I/O address is 0B0h With IOEXP low	o o bit 7 o—o bit 6 o o bit 5 o—o bit 4 o—o bit 3 o—o bit 2 o—o IOEXP	user defined	
W4	Select CPU RAM Memory Default is 2 kbyte	o o o o 2 kbyte	o o o o 8 kbyte	o o o o 16 kbyte
W5	Select CPU EPROM Memory Default is 8 kbyte	o o 8 kbyte	o o 16 kbyte	
W6	Spare PIO Bit Used for EEPROM if fitted	o o o not defined	o—o o high	o o—o low
W7	Spare PIO Bit Used for EEPROM if fitted	o o o not defined	o—o o high	o o—o low
W8	Select PCG Memory Default is 2 kbyte	o o—o o o—o 2 kbyte	o o—o o o—o 8 kbyte	o—o o o—o o 16 kbyte
W9	Select Keyboard Strobe Edge	o o—o +ve edge	o—o o -ve edge	
W10	Select Video and Attribute RAM Memory	o o 2 kbyte	o o 8 kbyte	
W11	Enable NMI from vert sync (for BWS-1158 Basic)	o o not connected	o—o connected	
W12	Reverse logic for horz sync pulse : BWS-2011 only	o—o o +ve logic	o o—o -ve logic	
W13	Reverse logic for vert sync pulse : BWS-2011 only	o—o o +ve logic	o o—o -ve logic	

Fig. 3-8: Link Selectable Options

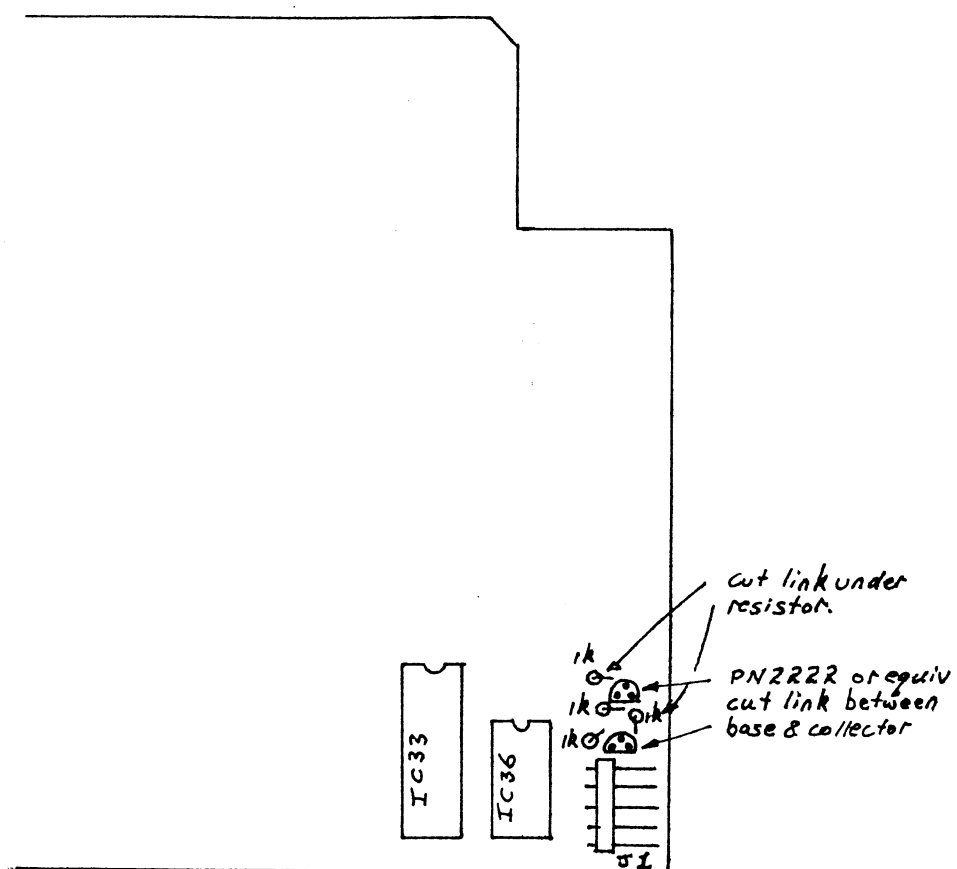


Fig. 3-9: TTL Video Output - Modifications to Invert Sync Pulse

3.3.4. EEPROM

Section not complete at time of printing.

4. TECHNICAL DESCRIPTION

4.1. Overview

The BWS-2010 Intelligent Video Display Card provides all the necessary circuitry to produce a stable flicker free display on a monochrome monitor. The BWS-2011 Intelligent Colour Video Display Card produces a similar quality display in colour.

The card has two major sections, one generating the video display from stored ASCII characters, and the other processing information received from the STD BUS to provide termulation emulation and store characters for display.

The video section of the card comprises a Motorola 6845 CRTC chip, video RAM, video attributes RAM, programmable character generator RAM and interfacing latches, shift registers and video logic. All video signals on the card are generated by the CRTC allowing flexible display generation and variations to the displayed picture size either by reprogramming the CRTC, adjusting the master clock crystal or both.

The processing section of the card comprises a Z80A microprocessor, associated EPROM and RAM, Z80A PIO and STD BUS interface logic. The processor provides the intelligence to emulate any desired terminal, manage graphics using semi-graphic characters and manage the type-ahead buffers for card input/output to the STD BUS.

The overall structure of the card is shown in Figure 4.1

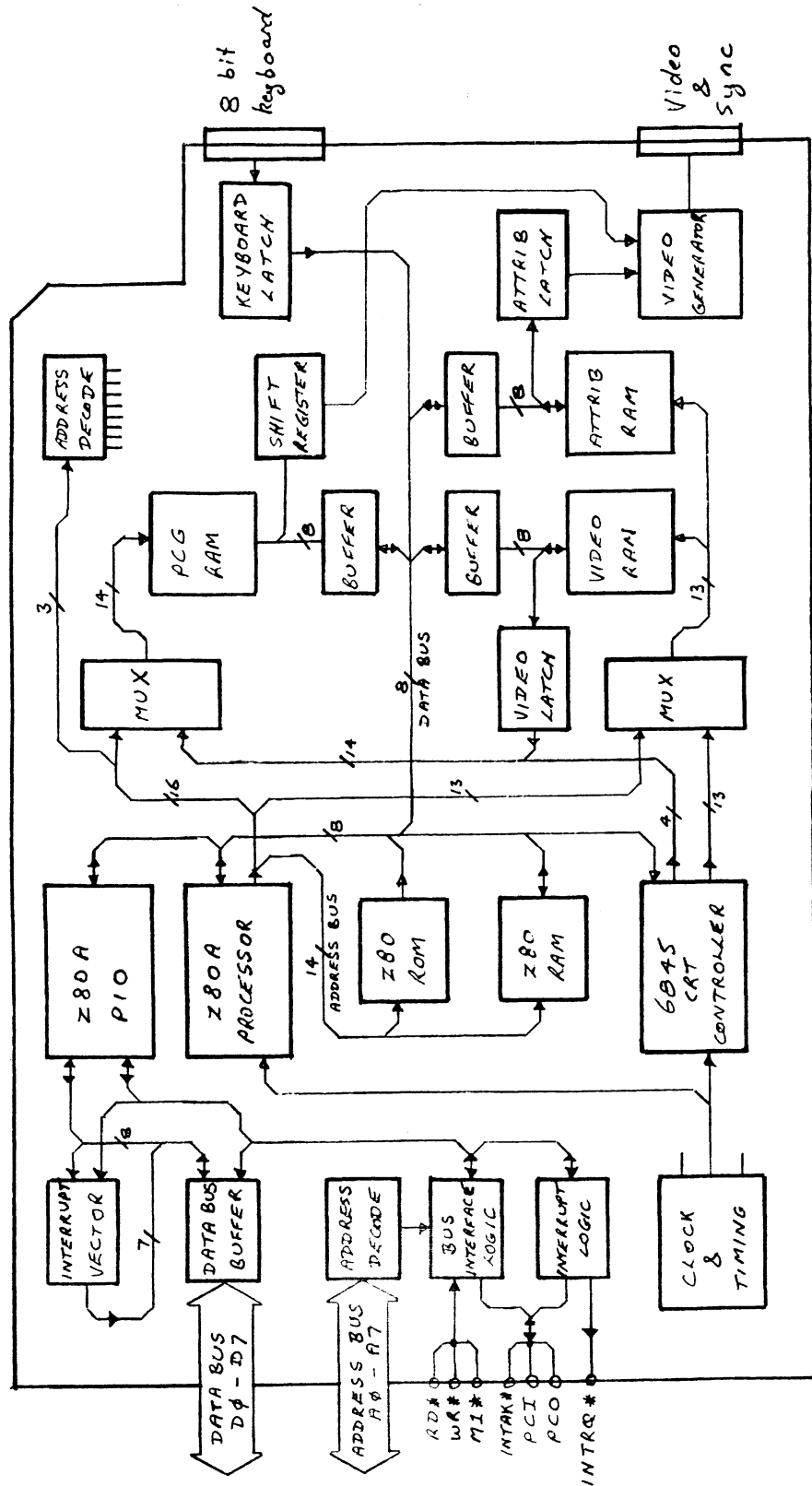


Fig. 4-1: BWS-2010/BWS-2011 Block Diagram

4.2. Hardware Description

4.2.1. Video Section

The video section comprises the 6845 CRTC controller, video RAM, Attribute RAM, PCG RAM, and various buffers, latches and shift registers, as shown in Fig 4-1. Its operation is as follows:

The main video clock signal is CCLK, which is generated from the nominally 13.5 MHz master clock through the clock PAL (BWS-2010C). The 6845 uses CCLK to generate the horizontal and vertical sync pulses, and the character address and row addresses.

The character cell addresses (row and column) pass through a set of 74LS157 multiplexers to the video and attributes RAM's. 13 address bits are supported, allowing up to 8 kbyte of video and attribute RAM to be accessed. This is equal to about 4 video pages.

8 bit data outputs from these RAM's are latched (to allow the Z80 to have access to the RAM's on the opposite clock cycle), and the video RAM output passes through another set of 74LS157 multiplexers to provide address bits for the Programmable Character Generator (PCG) RAM. Low order row bits from the 6845 complete the PCG address bits. Up to 16 kbyte of PCG RAM can be installed, as either RAM or EPROM.

Data output from the PCG RAM (the actual video bits) is latched into a shift register, and is then shifted into the video stream to make the next character row. Attribute bits are used to control the video bit stream within the video output PAL(s) as discussed below. Note that the attribute bits are one character ahead of the video data, and allowance must be made for this in the software which stores the attribute and video data in the video RAM's.

BWS-2010 Monochrome Video Generation

Monochrome video generation is done with a single PAL and a simple 3 stage resistive/diode OR arrangement. The video PAL (BWS-2010V) decodes the character attribute signals into 3 intensity bits, which are converted by pull-up resistors and diodes into the final intensity modulated video signal. Blanking and cursor signals from the 6845 are delayed 2 character widths (to match up with the correct character) and are added in using open collector exclusive-OR gates. Sync signals are included by using additional diodes with resistive thresholding, and the final composite video output is buffered by an emitter follower transistor with an output impedance of 75 ohm. Character flash is generated by a LM555 timer whose output is added in through the video PAL.

Separate sync signals are output directly from the 6845 CRTC controller. For negative logic sync signals, components to make a transistor inverter can be added to the card.

BWS-2011 Colour Video Generator

Colour video generation is done with two video PALs (BWS-2011V and BWS-2011R) and 74LS189 high speed bipolar RAMS. The PAL's decode the video attribute bits for each character into color RAM addresses, and the output of the colour RAMS become the video output from the card. The colour RAMS may be written to from the onboard Z80 processor, and hence act as a colour palette. (The colour palette RAMS can only be written into during the vertical sync pulse, to redefine a colour/attribute bit relationship from the available palette selection.)

Each colour RAM provides 4 bits of video output data. For TTL VDU's, only one colour RAM is required, to generate RGB and intensity bit streams. For analogue VDU's, three colour RAM's are used with the output of each RAM going to a high speed DAC to generate the final video output.

NOTE: The colour and monochrome video PALS are not interchangeable!

4.2.2. Processing Section

The processing section comprises clock generation, the Z80 microprocessor, the PIO, internal RAM and EPROM and the parallel keyboard interface.

Clock generation is done using a PAL (BWS-2011C) driven from the master crystal on the card (nominally 13.5 MHz). The clock PAL generates CCLK for the 6845 CRTIC, ZCLK for the Z80A processor, and some of the I/O enabling signals.

The oncard processor is a Z80A microprocessor chip running at 3.38 Mhz when the standard 13.5 MHz crystal is used. The Z80 has its own program memory comprising up to 16 kbyte of EPROM and up to 16 kbyte of RAM. ONLY THIS MEMORY CAN BE USED TO STORE Z80 PROGRAM, since the memory interleave cycle between the 6845 and the Z80 does not allow an opcode fetch to take place from video or PCG RAM.

Memory address decoding is done by a 74LS288 fuse link PROM, which generates various RAM enables as required. The memory map for the card is shown in Appendix A.

I/O addresses are only partially decoded, using dedicated I/O address lines to enable I/O devices. I/O device assignments are shown in Appendix A. No other I/O devices can be supported on the card, because of the partial I/O address decoding.

The PIO supports the STD BUS interface, providing a bi-directional 8 bit parallel interface between the bus and the Z80 processor. Spare PIO bits are used to program and read the EEPROM, blank the display and control the parallel keyboard interface. The PIO operates with port A in mode 2 and port B in mode 3 with interrupts masked off.

The parallel keyboard interface is provided using a 74LS374 octal latch, loaded from the incoming keyboard signal. A link-selectable transistor inverter is provided to allow the keyboard strobe to be either positive or negative logic. The keyboard strobe also sets a RS flip flop which read by the processor through the PIO. The flip flop is cleared when the main keyboard latch is read. The keyboard circuitry uses a RC differentiator to detect the leading edge of the keyboard strobe, and requires the keyboard to have valid data on the input at the start of the strobe signal.

4.2.3. STD BUS Interface

The video card occupies 4 I/O ports on the STD BUS out of 512 available I/O port addresses (8 bit decode plus IOEXP). The I/O address decoding is done with a 25LS2521 8 bit comparator, and can be mapped to any 4 bit boundary by adjusting links on the card.

Parallel data interchange to the STD BUS is through the PIO, operating in bi-directional mode 2 through port A. The status bits of the PIO are buffered on the STD BUS at bus address BASE+1 to provide status bits to the host processor on the bus.

Bus interface control is done with 2 PALS (BWS-2010B and BWS-2010I) which manage the parallel transfer of bytes between the bus and the card, and support interrupts. Registers in PAL BWS-2010I are used to latch the interrupt enable signals, and these signals are buffered back onto the bus at bus address BASE+1 to provide interrupt enable status bits.

The bus interface provides full vectored interrupt capability for data flowing to and from the video card. Interrupts may be generated when the card is ready to receive data, or has data to pass onto the host processor. Interrupt prioritisation is achieved using the PCI and PCO bus priority signals in the standard way. The interrupt priority signals are managed by the BWS-2010B PAL, which introduces approximately 25 ns delay in propagation. Standard Z80 timing allows for approximately 300 ns delay in total propagation delay of the interrupt priority signals, which means that at least 10 BWS-2010 video cards may be reliably used in a single STD BUS card frame, all operating in priority interrupt mode.

During an interrupt acknowledge cycle, the BWS-2010B PAL gates an interrupt vector from a 74LS374 latch onto the bus. The vector can be a single byte instruction opcode (Z80 mode 0), or it can be a 7 bit interrupt vector (Z80 mode 2, LSB = 0). In the latter case, bit 1 of the vector is defined by the interrupt PAL depending on whether it was a receive or transmit interrupt. This generates separate interrupt vectors for information flowing in either direction (similar to a Z80 DART).

NOTE: In most applications it is unnecessary to use the BWS-2010 video card in interrupt mode. For bytes sent to the card, the on-card handling of data clears the interface in approximately 30 microseconds (until the communications buffer is full). This corresponds to no more than 30 Z80 instruction executions, and most host application programs require more code than this to collect the next byte to output to the video card. Hence a simple check status and wait loop is sufficient in most circumstances.

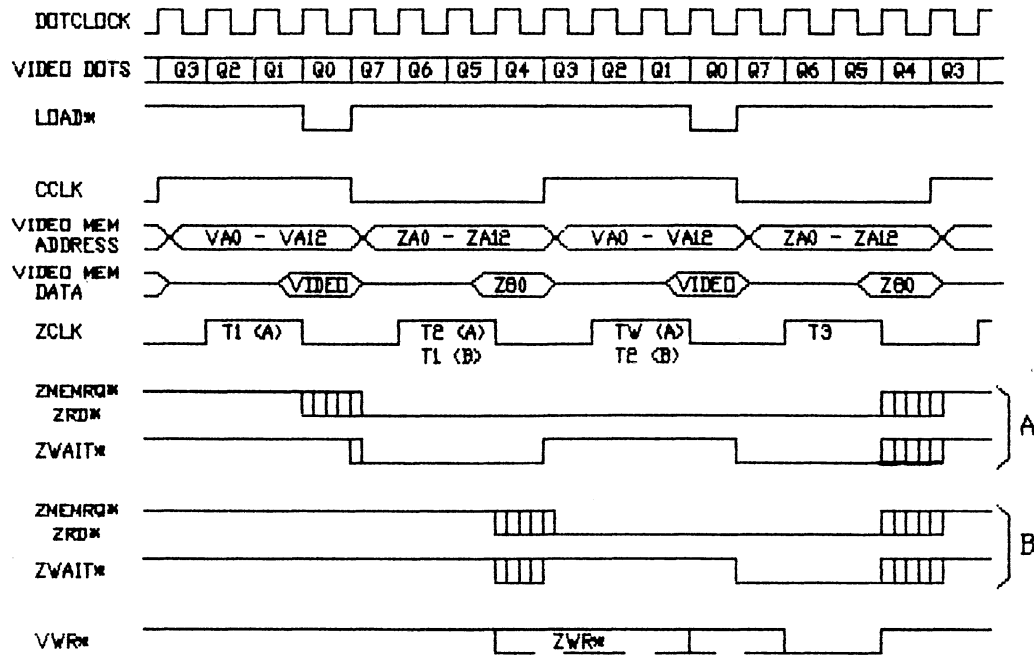
For bytes sent from the card (e.g. keyboard characters), these are buffered on card, and it is often acceptable to simply poll for more characters when convenient. Of course, interrupts must be used when a "break" type of data input is required.

4.2.4. Z80/CRTC Memory Interleave Timing

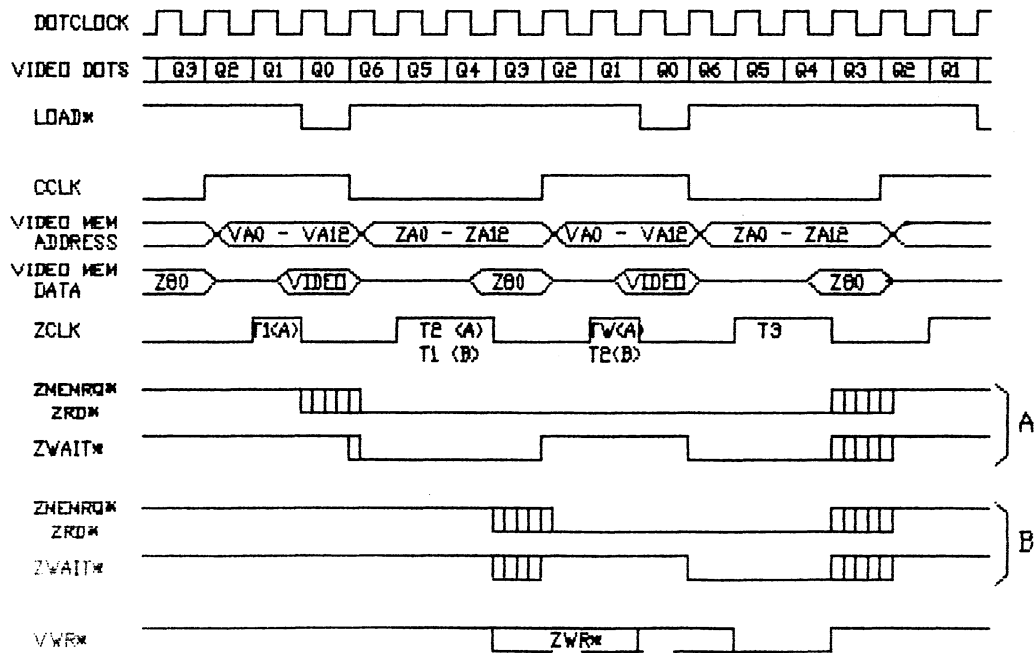
One of the main reasons for the extremely high rate of display that can be achieved with the BWS-2010 video card is the way in which the Z80 processor has access to the video memory. This is achieved by organising the Z80A and the 6845 CRTC to have access to video memory on opposite clock phases. Consequently, the Z80 can read and write to the video, attributes and programmable character generator memory at full processing speed, without waiting for horizontal or vertical sync blanking periods and without causing ANY flicker on the VDU screen.

Access to video memory is controlled by the BWS-2010C PAL. Signals ZCLK and CCLK are carefully synchronised as shown in Fig 4-2. The Z80 has access to video memory when CCLK is low and the CRTC has access to video memory when CCLK is high. ZCLK is arranged for the Z80 memory read and write strobe edge to occur when CCLK is low. Video data is extracted from video memory when CCLK is high, and is latched by the LOAD* pulse at the end of the high period of CCLK for subsequent character and video generation.

When the Z80 processor requires access to memory, it generates a ZMEMRQ* signal. If this access is to video memory (bit 15 high), the clock PAL generates a ZWAIT* signal until the next time that CCLK is low. The Z80 processor then completes its memory access. The maximum delay that can occur is one half cycle of CCLK, which is 300 ns.



8 VIDEO DOTS PER CHARACTER CELL



7 VIDEO DOTS PER CHARACTER CELL

Fig. 4-2: ZB0/CRTC Memory Interleave Timing Diagram

4.3. Internal Software Structure

Software for the BWS-2010/BWS-2011 video cards is designed in a highly modular fashion for maximum performance, reliability and flexibility. The software is written in three major sections, as follows.

The first software level is the terminal emulation, which is always supplied with the card. Both the on-board monitor (BWS-1008) and on-board Command Basic (BWS-1158) access the video memory, STD BUS interface and keyboard through the terminal emulation software.

The next software level is the optional Z80 monitor, which provides oncard assistance for debugging user written programs. The monitor interfaces to the terminal emulation software through a specially written BIOS.

The third software level is the optional Enhanced Command Basic, which uses some modules from the BWS-1008 Z80 monitor, and also accesses the terminal emulation through a specially written BIOS.

4.3.1. Terminal Emulation

The main loop of the terminal emulation software provides basic character handling, comprising checking the incoming characters against a set of Command Sequences, and placing the character into video memory if no sequence is detected. Control is passed to special subroutines through an indexed lookup table if a Command Sequence is found.

The STD BUS interface is managed by an interrupt service routine, which simply saves incoming bytes in a FIFO buffer. The main loop program then extracts these bytes at its leisure.

Keyboard handling is currently managed by a poll sequence within the main loop program. Characters entered from the keyboard are saved in an outgoing FIFO buffer, and are sent to the STD BUS interface by an interrupt service routine when requested by the receiving host computer.

Certain useful terminal emulation subroutines are also accessible directly through a jump table located at address 100h. These jump table entry points are listed in Figure 4-3 below.

All major data tables are moved to RAM when the card is initialised. This allows these tables to be modified and the card to be warm booted to a new state if desired by the user. For example, the 6845 can be reprogrammed by changing the setup parameters in RAM and jumping through location 103h. Section 4.3.4 describes the placement of the command tables and other sections of the terminal emulation software in EPROM and RAM memory.

Further internal details of the terminal emulation software are available on application to ByteWyde Systems.

Address (hex)	Label	Subroutine Function
0100	.vcold	Cold start - move EPROM tables to RAM
0103	.vwarm	Warm start - use existing tables in RAM
0106	.vmain	Jump to emulation main loop
0109	.vcinit	Initialise 6845 CRTC only - use RAM data
010C	.vioinit	Initialise I/O ports (PIO and all)
010F	.vvdunit	Initialise VDU pointers, attributes, etc
0112	.vvdud	Process byte in acc A through VDU driver
0115	.vkeyst	Check keyboard status
0118	.vkeyin	Get character from keyboard
011B	.vcinst	Check PIO status for character input
011E	.vcin	Get character from PIO
0121	.vcost	Check PIO status for character output
0124	.vcout	Send character to PIO

Fig. 4-3: Terminal Emulation Jump Table

4.3.2. Oncard Z80 Monitor (BWS-1008)

The oncard monitor is a modified version of ByteWyde Systems standard BWS-1000 Z80 monitor program. The monitor is intended to provide a support environment for the development of special oncard software, or to allow users to investigate the detail operation of the card. Two additional functions have been included, being a "Send to screen" function (an effective LOCAL function), and an "Absolute terminal" function, which jumps to the terminal software described in Section 4.3.1 above. The BWS-1008 monitor does not support hardware address match interrupts or multiple loop program breakpoints.

The monitor software is completely separate from the terminal emulation software, and interfaces through a specially written BIOS module. The VDU/Keyboard are used as the "console" device, and the STD BUS interface is the "remote" device.

Further details on the monitor program are available in the BWS-1000 standard manual, which may be purchased separately on request.

4.3.3. Oncard Enhanced Command Basic

The BWS-1158 is a completely standard implementation of ByteWyde Systems "Enhanced Command Basic" currently being sold as BWS BASIC by Pro-Log under license from ByteWyde Systems. (The version supplied in the video card is the latest revision which has some additional features over the Pro-Log release).

The implementation uses a special BIOS module to interface to the terminal emulation software (similar to the Z80 monitor software). The VDU/Keyboard are used as the "console" device, and the STD BUS interface is the "remote" device. Basic uses the vertical sync pulse as the basic timing interval. This is acceptable for multitasking, but means that the long term time-of-day-clock stability is not good.

Further details are available in the BWS-1150 manual, which may be purchased separately on request.

4.3.4. Software Memory Map

CPU EPROM -	0000	-----	
		Hardware Jump Vectors	
	0080	-----	
		Z80 Monitor Jump Table	(BWS-1008 only)
	00C0	-----	
		Extended Jump Table	(BWS-1158 only)
	0100	-----	
		Terminal Emulation Jump Table	

		Terminal Emulation Software Modules	
	0800	-----	
		BWS-1008 Z80 Monitor Software Modules	(BWS-1008 only)
	0B00	-----	
		Command Basic Jump Table	(BWS-1158 only)

CPU RAM		Command Basic Software Modules	
	1800	-----	
		Character Set (Default)	
	2000	-----	
		Character Set (BWS-1158)	(BWS-1158 only)
	3000	-----	
		Autostart Program for Command Basic (BWS-1158)	
	/	/	
	4000	-----	
		DATA BUFFER FROM STD BUS	
	4100	-----	
		DATA BUFFER TO STD BUS	
	4200	-----	
		VDU DRIVER SCRATCH RAM	
	4210	-----	
		Z80 Mode 2 vector Table	
	4218	-----	
		Current 6845 Setup Constants	
	4228	-----	
		vsync per sec (for BWS-1158)	
	4229	-----	
		Current PIO Setup Constants	
	4235	-----	
		Current Colour RAM Setup	(BWS-2011 only)
	4270	-----	
		Terminal Emulation Tables	
	4300	-----	
		BWS-1008 Scratch RAM	
	4480	-----	
		BWS-1158 Scratch RAM	
	4800	-----	
		BWS-1158 Program Buffer	
	/	/	

5. APPLICATION NOTES

5.1. Interrupts

Not available at time of printing

5.2. User Programming

Not available at time of printing

5.3. Co-processing using BWS-1100 Video Cards

Not available at time of printing

6. MAINTENANCE

6.1. Warranty

The BWS-2010 Intelligent Video Card and the BWS-2011 Intelligent Colour Video Card are guaranteed against all electrical and mechanical defects found to be due to faulty workmanship or components within the first 90 days after delivery. Faulty cards will be repaired without charge within this period if the card is returned to ByteWyde Systems, or to the dealer from whom the card was purchased. This warranty does not include the cost of packing and postage of the faulty card to and from the repair location.

This warranty is expressly declared void if a card is found to be damaged due to improper use or mishandling. In particular, mechanical damage due to careless handling, or electrical damage due to overvoltages or misconnections being applied to the video and keyboard connectors, void the above warranty.

This warranty extends only to the repair or making good of BWS-2010 and BWS-2011 video cards purchased from ByteWyde Systems or any authorised dealer. NO CLAIMS FOR CONSEQUENTIAL DAMAGES OF ANY KIND WILL BE CONSIDERED. The warranty expressed in this manual expressly excludes any damages or losses of any kind (including loss of income) that may be claimed to have arisen as a consequence of a failure of the product.

6.2. Maintenance

After the warranty period has expired, ByteWyde Systems offer a maintenance service on a cost plus basis. Where possible, hardware which cannot be directly repaired within 48 hours after receipt by ByteWyde Systems will be repaired on an exchange basis.

A. On-Card Memory and I/O Map

		FFF hex	Not Available	E1
Video Attributes			Keyboard Latch	E0
		E000 hex	Cursor Colours	DC
Video Characters			Background Colours	D8
		C000 hex	Foreground Colours	D0
Programmable Character Set				
		8000 hex	Not Available	82
CPU RAM Memory			Z80A PIO	80
		4000 hex	Not Available	42
CPU EPROM Memory			6845 CRTC	40
		0000 hex	Not Available	

Fig. A-1: BWS-2010 Memory and I/O Address Map

E0 Keyboard Data Latch

D0-D7 Foreground Colours (data byte = 2x for COLOUR RAM 1)
D8-DB Background Colours (data byte = 4x for COLOUR RAM 2)
DC-DF Cursor Colours (data byte = 8x for COLOUR RAM 3)

80 PIO Data Port A
81 PIO Control Port A
82 PIO Data Port B
83 PIO Control Port B

40 CRTC Address Register
41 CRTC Data Register

Fig. A-2: On-Card I/O Port Allocation

Blank	Keyin	spare	bell	spare	spare	vsync	busy
7	6	5	4	3	2	1	0

Fig. A-3: PIO Port B Bit Usage

B. STD BUS Interface Summary**B.1. I/O Port Map**

STD BUS I/O Address	I/O Port Function	R/W or R/O
BASE	Data Port	R/W
BASE+1	Control/Status Port	R/W
BASE+2	Interrupt Vector Port	R/W

B.2. Port Bit Usage Summary**Control/Status Port Bit Usage Summary**

x	x	Busy	x	TxE	RxE	TxR	RxR
7	6	5	4	3	2	1	0

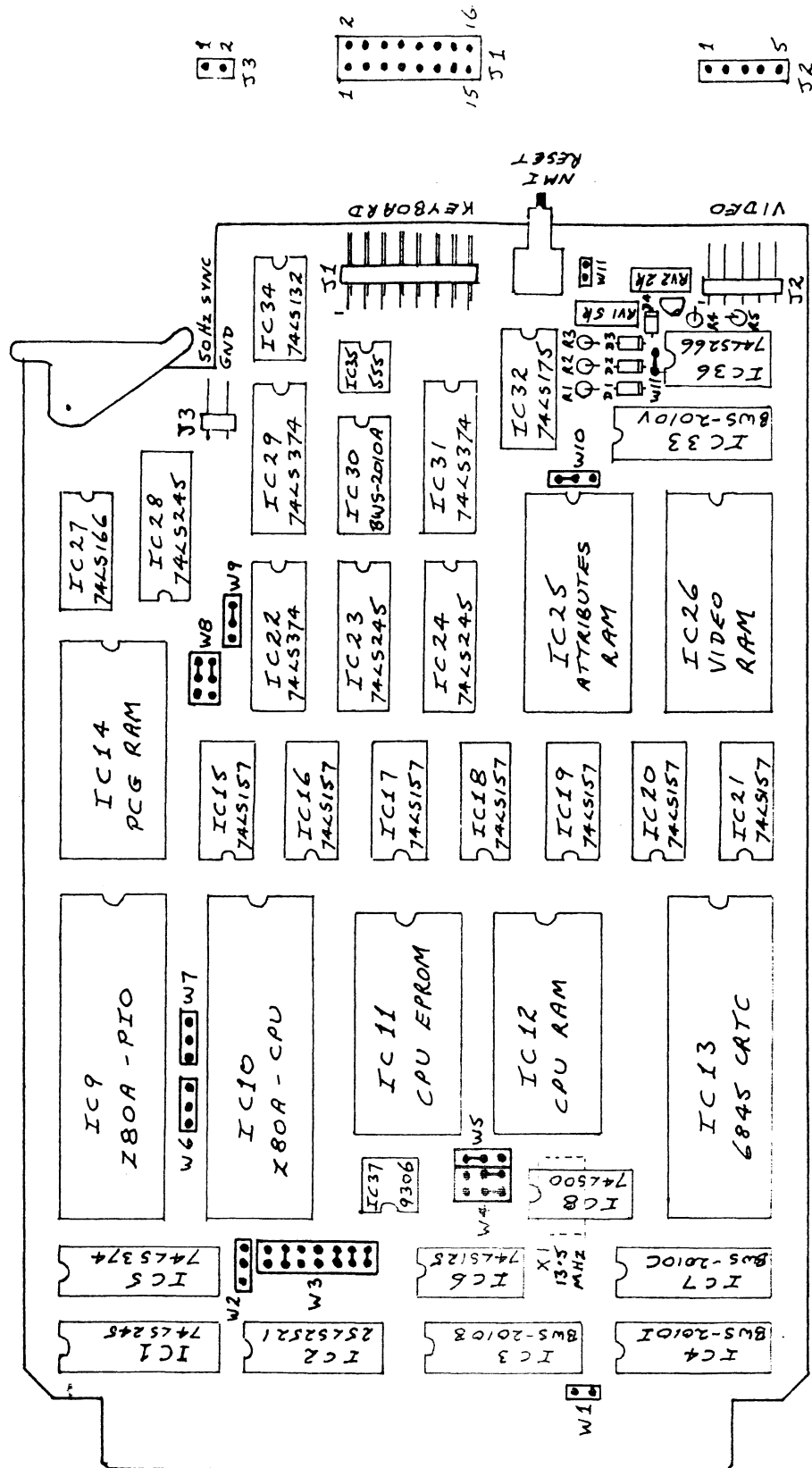
RxR = data byte ready to send to STD BUS (high = ready)
 TxR = ready to receive data byte from STD BUS (high = ready)
 RxE = Interrupts enabled for RxR (high = enabled)
 TxE = Interrupts enabled for TxR (high = enabled)
 Busy = Video Card Busy (high = busy)

Interrupt Vector Port Bit Usage Summary

h	h	h	h	h	h	i	h
7	6	5	4	3	2	1	0

h = bit set by host via write to vector port
 i = bit set by host port write or by interrupting device depending on link W2.
 Set to 0 for TxR interrupt) If W2 linked as 
 Set to 1 for RxR interrupt) Refer to Section 3.3

C. Reference Drawings



END ON VIEW

Fig. C-1: BWS-2010 Video Card - Component Layout Diagram

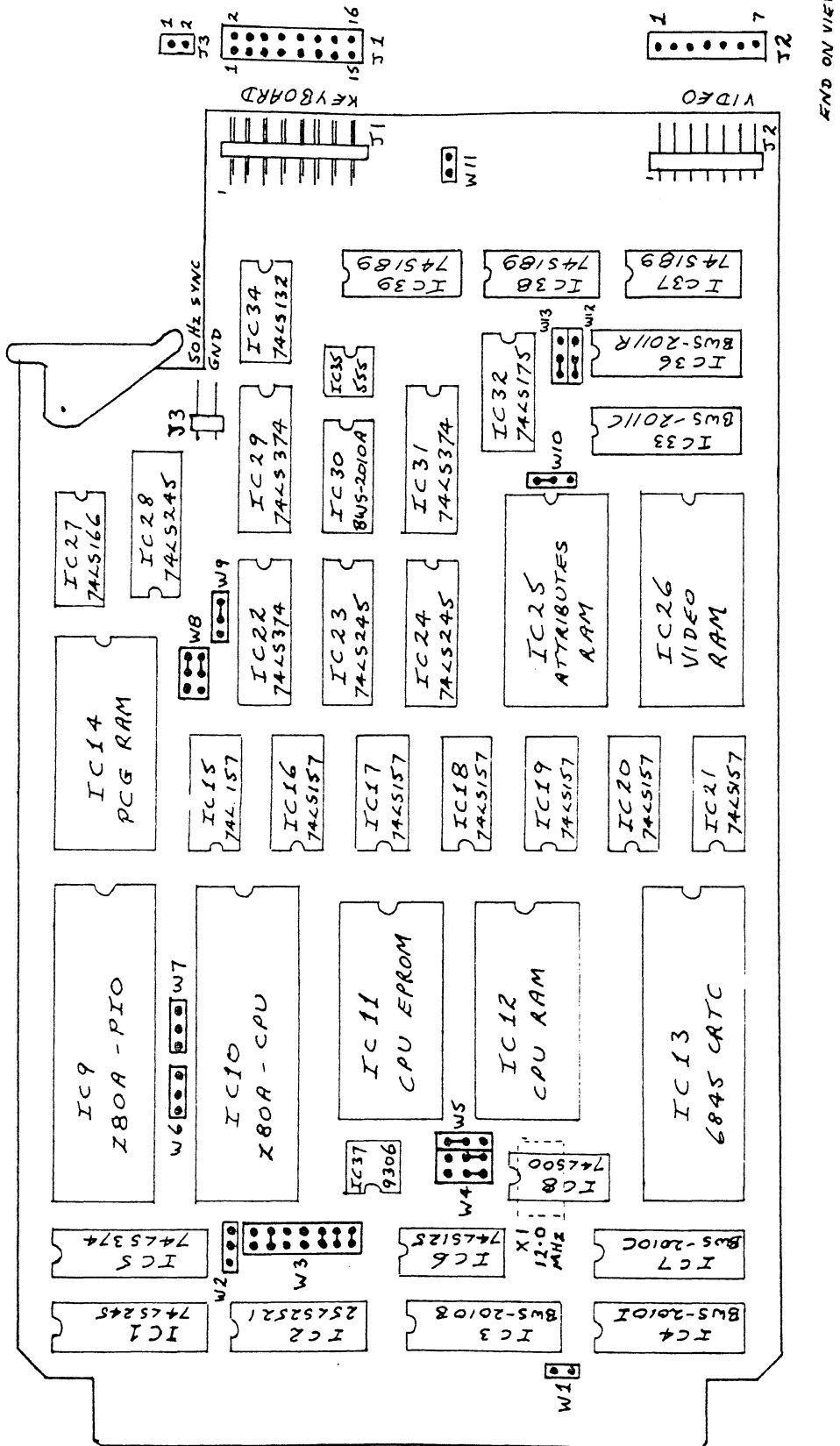
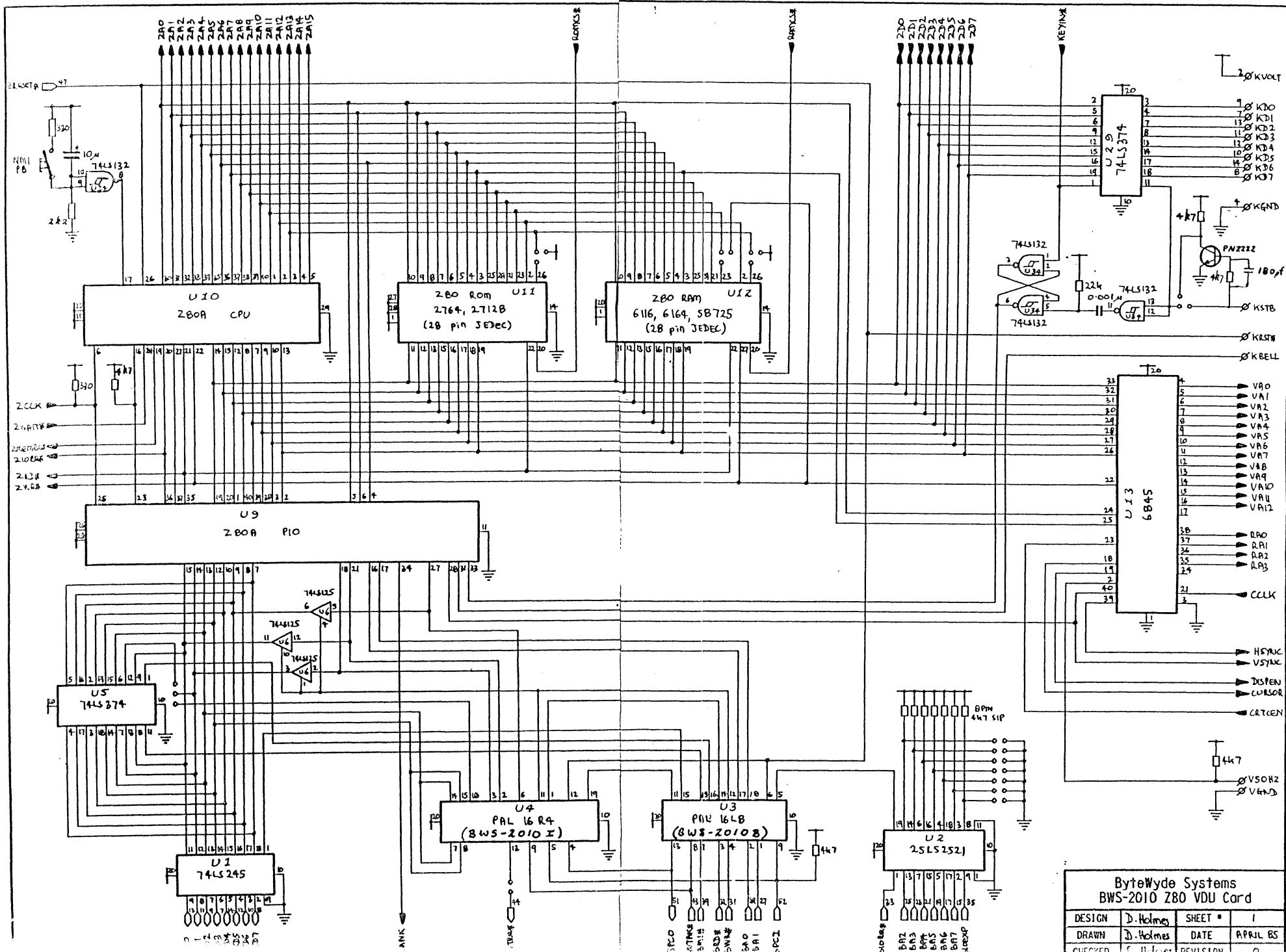


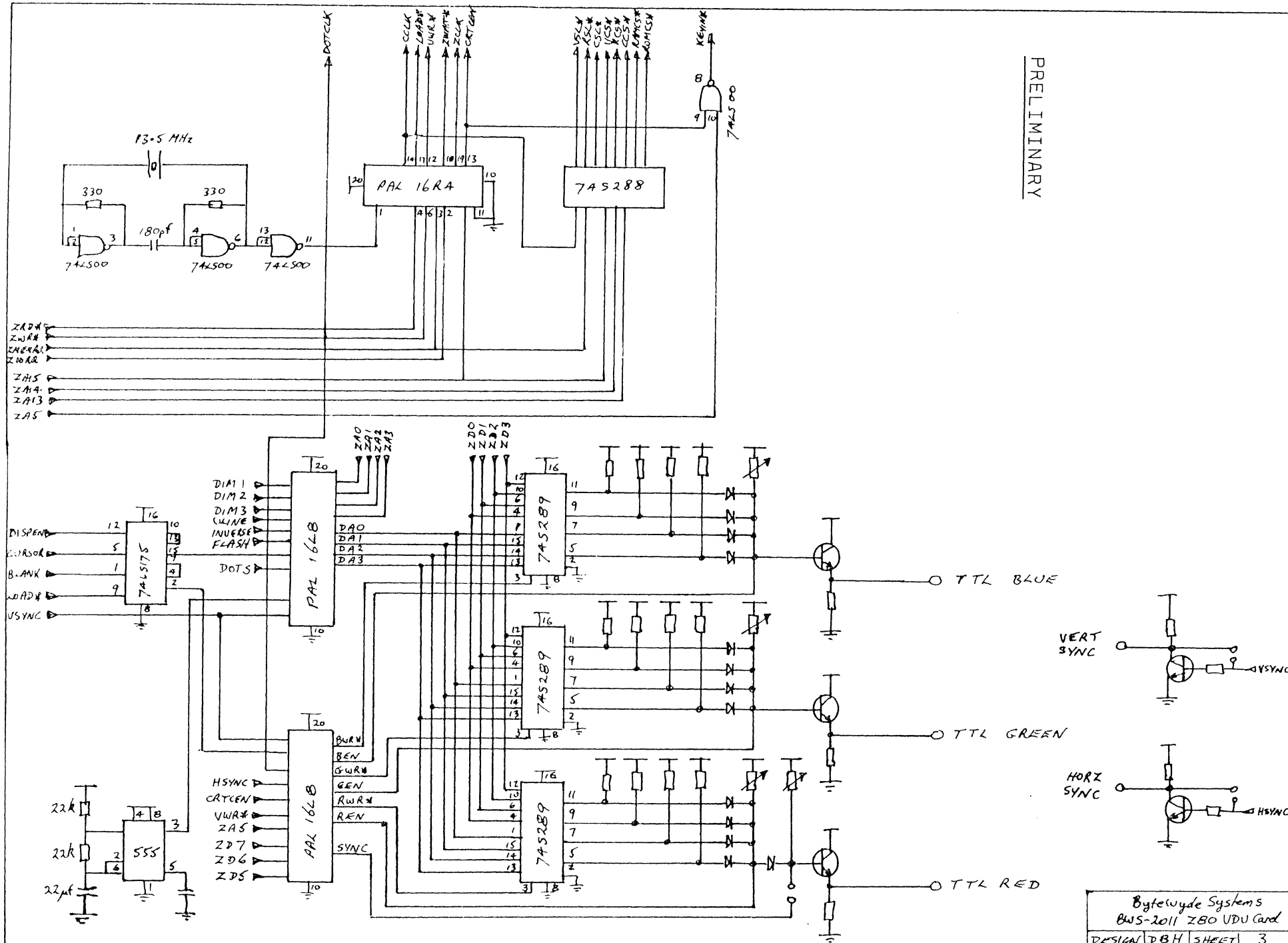
Fig. C-2: BWS-2011 Video Card - Component Layout Diagram



ByteWyde Systems			
BWS-2010 Z80 VDU Card			
DESIGN	D. Holmes	SHEET	1
DRAWN	D. Holmes	DATE	APRIL 83
CHECKED	D. Holmes	REVISION	0

PRELIMINARY

C.6



ByteWyde Systems			
BWS-2011 Z80 VDU Card			
DESIGN	DBH	SHEET	3
DRAWN	DGH	DATE	JUNE 85
CHECKED		REV.	

D. Summary of Terminal EmulationsD.1. ADM31A Emulation

control ^	Cursor home
control G	Ring keyboard bell
control H	Cursor left one character
control J	Cursor down one line
control K	Cursor up one line
control L	Cursor right one character
control M	Cursor to start of line
control Z	Clear screen
ESC (1) Select brightness 0	ESC (1) Select foreground colour 0
ESC (2) Select brightness 1	ESC (2) Select foreground colour 1
ESC (3) Select brightness 2	ESC (3) Select foreground colour 2
ESC (4) Select brightness 3	ESC (4) Select foreground colour 3
ESC (5) Select brightness 4	ESC (5) Select foreground colour 4
ESC (6) Select brightness 5	ESC (6) Select foreground colour 5
ESC (7) Select brightness 6	ESC (7) Select foreground colour 6
ESC (8) Select brightness 7	ESC (8) Select foreground colour 7
ESC < Dim video on	ESC (9) Select background colour 0
ESC (Normal brightness	ESC (A) Select background colour 1
ESC > Bright video on	ESC (B) Select background colour 2
ESC { Underline off	ESC (C) Select background colour 3
ESC } Underline on	
ESC [Inverse video off	
ESC] Inverse video on	

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ESC :	Flashing video on	ESC D	Cursor Left
ESC ;	Flashing video off	ESC = Y X	Direct cursor addressing
ESC m	Cursor OFF	ESC H	Cursor Home
ESC #	Display ON	ESC A	Cursor Up
ESC \$	Display OFF	ESC B	Cursor Down
ESC x	Cursor ON	ESC C	Cursor Right
ESC T			Erase to end of line
ESC *			Clear to end of screen
ESC v			Clear Screen
ESC E			Insert line
ESC R			Delete line
ESC 0			Select character set 0
ESC 1			Select character set 1
ESC 2			Select character set 2
ESC 3			Select character set 3
ESC h			Hex load
ESC c			Hex load to Color RAM
ESC g nnnn			Jump to Address nnnn

D. Summary of Terminal Emulations

D.2. VT52 Emulation

Not complete at time of printing

D. Summary of Terminal Emulations

D.3. VT100 Emulation

Not complete at time of printing